CLAIM AMENDMENTS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip having a central circuit area at which a high noise resistivity circuit is formed, a peripheral circuit area surrounding the central circuit area, and a low noise resistivity circuit being formed in the peripheral circuit area;

a second semiconductor chip which is mounted on the central circuit area of the first semiconductor chip;

a first electrode group which is formed on an area between the central circuit area and the peripheral circuit area of the first semiconductor chip ~~and arranged along an outer periphery of the first semiconductor chip in such a manner as to surround the second semiconductor chip~~;

a second electrode group which is formed on an outer area of the peripheral circuit area of the first semiconductor chip ~~and arranged along the outer periphery of the first semiconductor chip in such a manner as to surround the first electrode group~~;

a third electrode group which is formed on the second semiconductor chip;

a plurality of first wires for electrically connecting the first electrode group and the third electrode group to each other; and

external connection terminals which are electrically connected to the second electrode group;

~~wherein the first semiconductor chip comprises a first circuit element region which is surrounded by the first electrode group, and a second circuit element region which surrounds the first electrode group and is surrounded by the second electrode group~~.

2. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip having a first circuit element region at which a high noise resistivity circuit is formed, and a second circuit element region at which a low noise resistivity circuit is formed, and which is positioned between the first circuit element region and an outer periphery;

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a plurality of first electrodes which are formed on the first semiconductor chip and arranged in a region between the first circuit element region and the second circuit element region;

a plurality of second electrodes which are formed on the first semiconductor chip and arranged in a region between the second circuit element region and the outer periphery;

a second semiconductor chip which is mounted in the first circuit element region of the first semiconductor chip;

a plurality of third electrodes which are formed on the second semiconductor chip;

a plurality of first wires for electrically connecting the first electrodes and the third electrodes to each other; and

external connection terminals which are electrically connected to the second electrodes.

3. (Original) The semiconductor device according to claim 1, wherein:

the external connection terminals are conductive leads;

the plurality of leads are arranged along the outer periphery of the first semiconductor chip at positions separate from the first semiconductor chip by a predetermined distance; and

the second electrode group and the leads are electrically connected to each other by a plurality of second wires.

4. (Original) The semiconductor device according to claim 1, wherein a size of the second semiconductor chip is smaller than that of the first semiconductor chip.

5. (Original) The semiconductor device according to claim 1, wherein the first semiconductor chip and the second semiconductor chip are sealed with a resin.

6. (Original) The semiconductor device according to claim 1, wherein:

the external connection terminals are conductive leads;

the plurality of leads are arranged along the outer periphery of the first

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semiconductor chip at positions separate from the first semiconductor chip by a predetermined distance;

the second electrode group and the leads are electrically connected to each other by a plurality of second wires;

the first semiconductor chip and the second semiconductor chip are sealed with a resin; and

the first wires and the second wires are sealed with the resin.

7. (Original) The semiconductor device according to claim 1, wherein the first semiconductor chip is formed on a support.

8. (Original) The semiconductor device according to claim 1, wherein the first electrode group and the second electrode group are formed along sides of the outer periphery of the first semiconductor device.

9. (Original) The semiconductor device according to claim 1, wherein the third electrode group is formed along an outer periphery of the second semiconductor chip.

10. (New) A semiconductor device comprising:

a first semiconductor chip having a central circuit area on which a high noise resistivity circuit is formed, a peripheral circuit area surrounding the central circuit area, on which a low noise resistivity circuit is formed, a first electrode area located between the central circuit area and the peripheral circuit area and a second electrode area located at outside of the peripheral circuit area;

a second semiconductor chip mounted on the central circuit area of the first semiconductor chip;

a plurality of first electrodes formed on the first electrode area of the first semiconductor chip;

a plurality of second electrodes formed on the second electrode area of the first semiconductor chip;

a plurality of third electrodes formed on the second semiconductor chip;

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a plurality of electrical connections for electrically connecting the first electrodes and the third electrodes, respectively; and

a plurality of external connection terminals electrically connected to the second electrodes, respectively.

11. (New) The semiconductor device according to claim 10, wherein a size of the second semiconductor chip is smaller than that of the central circuit area of the first semiconductor chip.

12. (New) The semiconductor device according to claim 10, wherein the low noise resistivity circuit includes an analog circuit.

13. (New) The semiconductor device according to claim 10, wherein the first and second semiconductor chips are sealed with a resin.

14. (New) The semiconductor device according to claim 10, wherein the electrical connections are a plurality of wires.

15. (New) The semiconductor device according to claim 10, wherein external connection terminals are electrically connected to the second electrodes by a plurality of wires.

16. (New) The semiconductor device according to claim 1, wherein a size of the second semiconductor chip is smaller than that of the central circuit area of the first semiconductor chip.

17. (New) The semiconductor device according to claim 1, wherein the low noise resistivity circuit includes an analog circuit.

18. (New) The semiconductor device according to claim 2, wherein a size of the second semiconductor chip is smaller than that of the central circuit area of the first semiconductor chip.

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19. (New) The semiconductor device according to claim 2, wherein the low noise resistivity circuit includes an analog circuit.

20. (New) The semiconductor device according to claim 2, wherein the first and second semiconductor chips are sealed with a resin.

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